AMENDMENT TO THE CLAIMS

1. (Currently Amended) A ~~processor~~ system comprising:

a central processing unit;

a writable memory;

means for external communication;

operation mode selection means for selecting an operation mode; and

control means for stopping the operation of said central processing unit, mapping to an address area in said writable memory which includes a start address at which said central processing unit is to start reading upon resuming operation, and writing to said memory starting at the start address an IPL program received ~~transferred~~ from an external source ~~the outside~~ through said communication means when an IPL operation mode is selected by said operation mode selection means, and for thereafter resuming ~~canceling the stoppage of the~~ operation of said central processing unit such that said central processing unit reads said memory from the start address and initiates ~~; and IPL operation means for executing~~ the IPL program written to said memory from the external source. ~~through the operation of said central processing unit to download a system program.~~

2. (Currently Amended) A ~~processor~~ system according to claim 1, wherein said control means includes:

mapping control means for mapping said writable memory to an area including an address which said central processing unit first reads immediately after startup in the IPL operation mode; and

write control means for controlling writing of the IPL program such that the writing starts from the address read first.

3. (Currently Amended) A ~~processor~~ system according to claim 1, wherein said control means includes:

detection means for detecting a situation where transfer of the IPL program should be terminated; and

termination processing means for terminating writing to said memory when a situation where the transfer should be terminated is detected by said detection means.

4. (Currently Amended) A ~~processor~~ system according to claim 3, wherein said detection means detects a situation where the transfer should be terminated by ascertaining that a transferred data amount set in advance has been reached.

5. (Currently Amended) A ~~processor~~ system according to claim 3, wherein said detection means detects a situation where the transfer should be terminated by detecting from transferred data a code designating termination of transfer.

6. (Currently Amended) A ~~processor~~ system according to claim 1, wherein said control means includes bus control means for changing a connection of a bus according to the operation mode, and the bus control means changes the memory as an IPL program writing destination according to the operation mode.

7. (Currently Amended) A ~~processor~~ system according to claim 1, wherein said control means performs control such that a check program for checking the operation or condition of a certain device is written to said memory together with the IPL program, and the check program is executed when said central processing unit starts operating.

8. (Currently Amended) A ~~processor~~ system according to claim 7, wherein the check program is a program for checking the operation of a peripheral device connected to the ~~processor~~ system.

9. (Currently Amended) A ~~processor~~ system according to claim 7, wherein the check program is a program for checking the state of a memory connected to the ~~processor~~ system.

10. (Currently Amended) A ~~processor~~ system according to claim 7, wherein the check program is a program for checking the state of connection of a peripheral device connected to the ~~processor~~ system.

11. (Currently Amended) A method of starting a ~~processor~~ system having a central processing unit, a writable memory, and a communication ~~portion~~ unit for external communication, said method comprising the steps of:

stopping ~~the~~ operation of the ~~said~~ central processing unit when an IPL

operation mode is selected;

mapping to an address area in the writable memory which includes a start address at which the central processing unit is to start reading upon resuming operation;

writing to the memory starting at the start address ~~said memory~~ an IPL program received ~~transferred~~ from an external source ~~the outside~~ through said communication ~~portion~~ unit; and

resuming ~~canceling the stoppage of the~~ operation of the ~~said~~ central processing unit after ~~said~~ writing the IPL program to the memory, such that the central processing unit reads from the start address and initiates ~~; and executing~~ the IPL program written to the ~~said~~ memory from the external source. ~~through the operation of said central processing unit to download a system program.~~

12. (Original) A method according to claim 11, wherein said writable memory is mapped to an area including an address which said central processing unit first reads immediately after startup in the IPL operation mode, and said writing of the IPL program is controlled so as to start from the address read first.

13. (Original) A method according to claim 11, wherein a situation where transfer of the IPL program should be terminated is detected, and said writing to said memory is terminated when a situation where the transfer should be terminated is detected.

14. (Original) A method according to claim 13, wherein a situation

where the transfer should be terminated is detected by ascertaining that a transferred data amount set in advance has been reached.

15. (Original) A method according to claim 13, wherein a situation where the transfer should be terminated is detected by detecting from transferred data a code designating termination of transfer.

16. (Original) A method according to claim 11, wherein the memory used as an IPL program writing destination is changed according to the operation mode by changing a connection of a bus according to the operation mode.

17. (Original) A method according to Claim 11, wherein control is performed such that a check program for checking the operation or condition of a certain device is written to said memory together with the IPL program, and the check program is executed when said central processing unit starts operating.

18. (Currently Amended) A method according to claim 17, wherein the check program is a program for checking the operation of a peripheral device connected to the ~~processor~~ system.

19. (Currently Amended) A method according to claim 17, wherein the check program is a program for checking the state of a memory connected to the ~~processor~~

system.

20. (Currently Amended) A method according to claim 17, wherein the check program is a program for checking the state of connection of a peripheral device connected to the ~~processor~~ system.